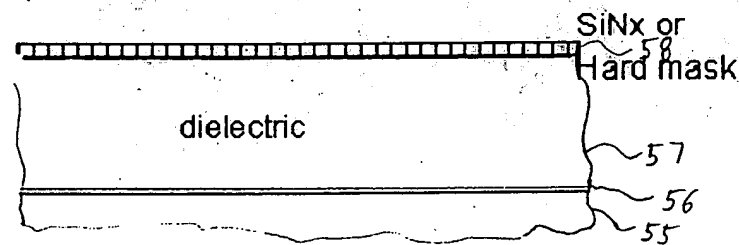


Figure 1 - Overall diagram of a copper interconnection structure

Process sequence 1: Single Damascene

Deposited dielectric materials



Resist patterning & RIE

FIG 2A

etch via holes or lines

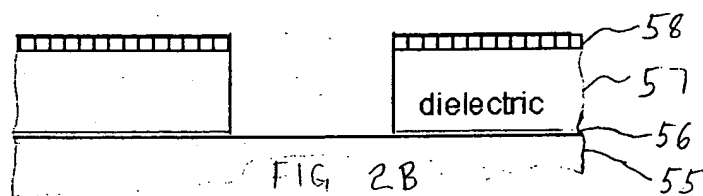


FIG 2B

Fill metals & CMP to remove excess metals

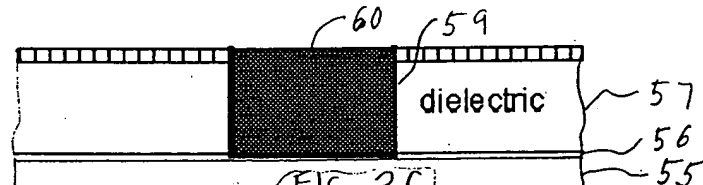


FIG 2C

Selective electroless deposition capping layer on top of Cu

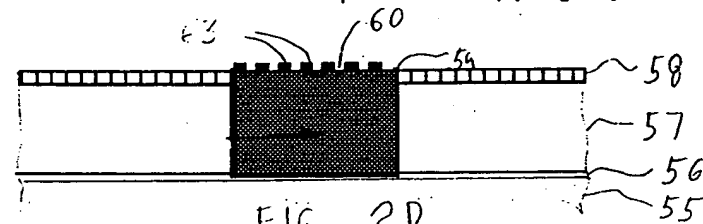
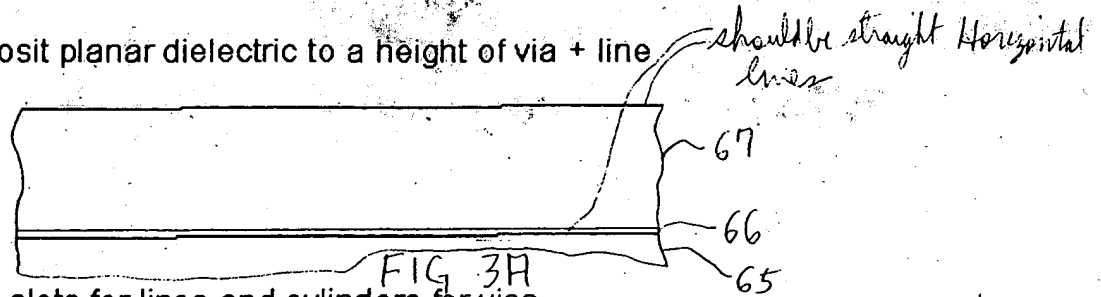


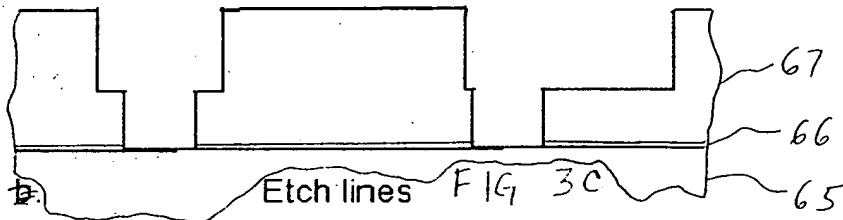
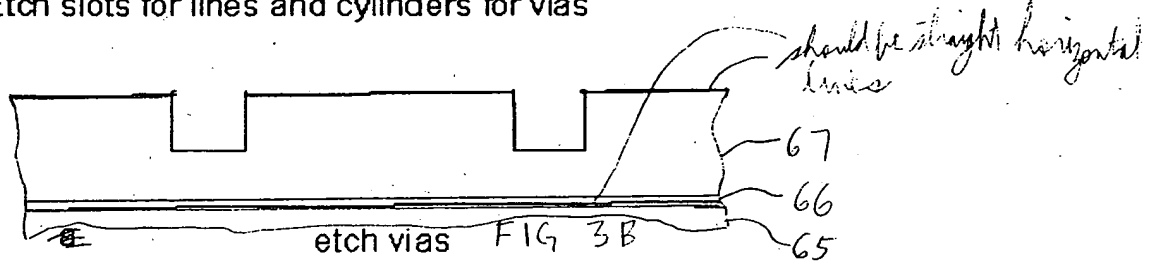
FIG 2D

Process sequence 2: Dual Damascene

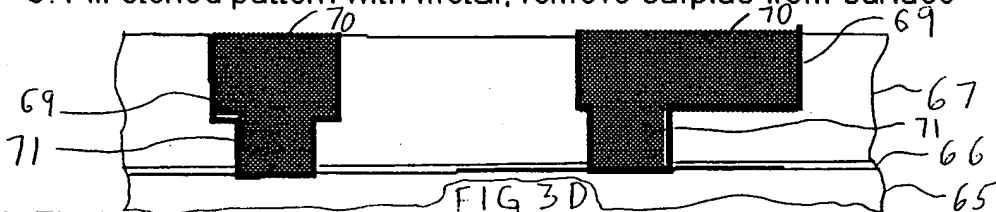
1. Deposit planar dielectric to a height of via + line



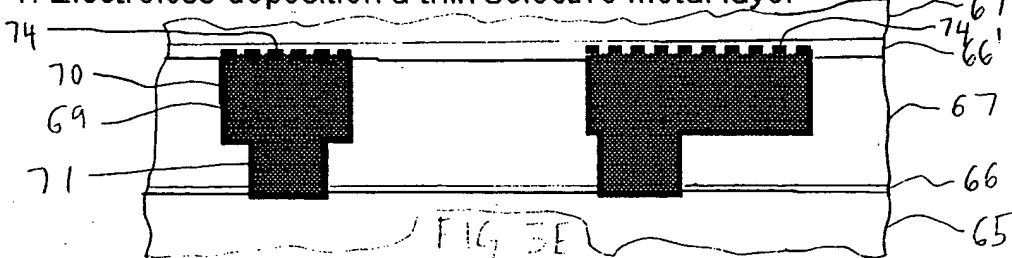
2. Etch slots for lines and cylinders for vias



3. Fill etched pattern with metal, remove surplus from surface



4. Electroless deposition a thin selective metal layer



75

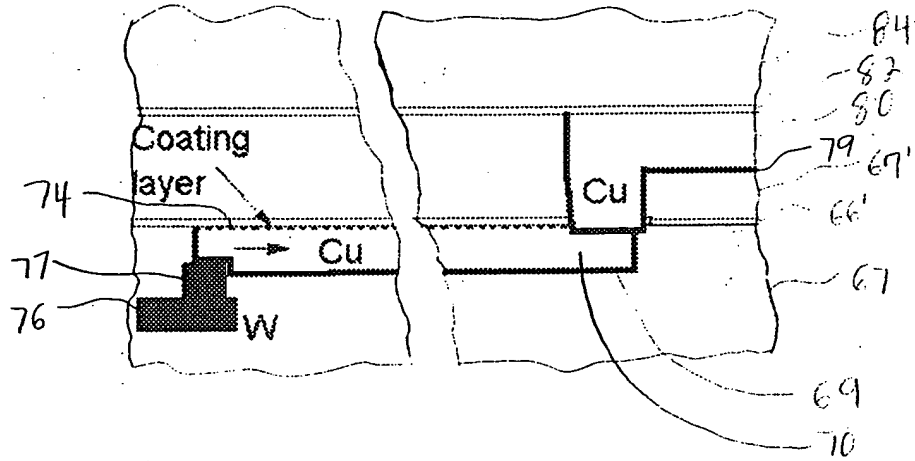


FIG 4

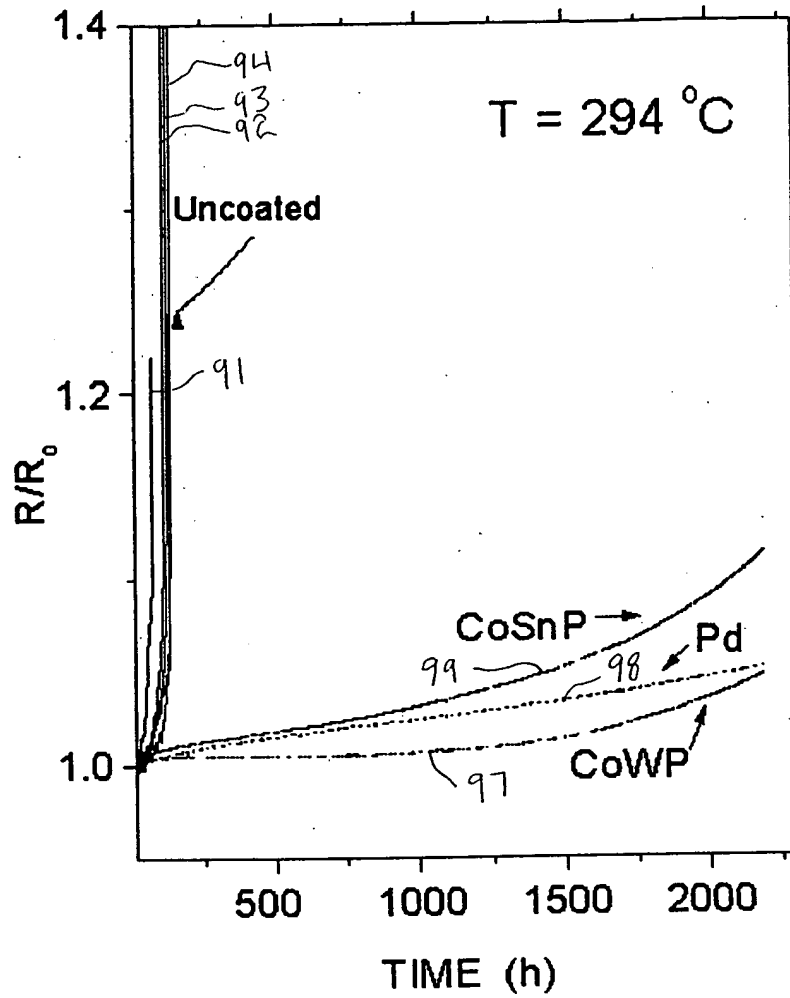


FIG 5